Tunable Charge-Trap Memory Based on Few-Layer MoS_2

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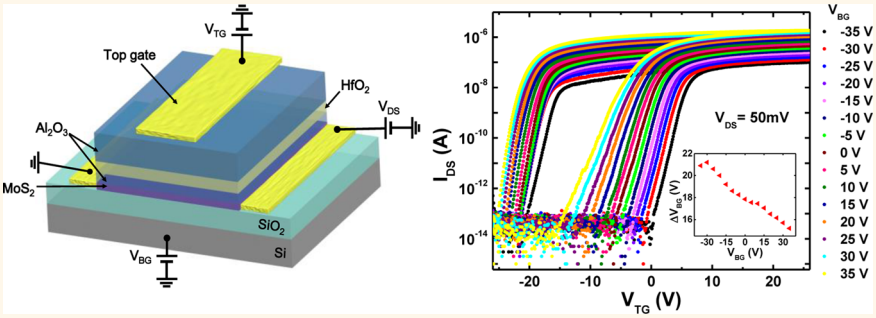
ABSTRACT



Charge-trap memory with high-κ dielectric materials is considered to be a promising candidate for next-generation memory devices. Ultrathin layered two-dimensional (2D) materials like graphene and MoS_2 have been receiving much attention because of their fantastic physical properties and potential applications in electronic devices. Here, we report on a dual-gate charge-trap memory device composed of a few-layer MoS_2 channel and a three-dimensional (3D) $Al_2O_3/HfO_2/Al_2O_3$ charge-trap gate stack. Because of the extraordinary trapping ability of both electrons and holes in HfO_2, the MoS_2 memory device exhibits an unprecedented memory window exceeding 20 V. Importantly, with a back gate the window size can be effectively tuned from 15.6 to 21 V; the program/erase current ratio can reach up to 10^4, allowing for multibit information storage. Moreover, the device shows a high endurance of hundreds of cycles and a stable retention of ~28% charge loss after 10 years, which is drastically lower than ever reported MoS_2 flash memory. The combination of 2D materials with traditional high-κ charge-trap gate stacks opens up an exciting field of nonvolatile memory devices.

KEYWORDS: charge-trap memory · MoS_2 · memory window · dual gate · memory characteristics

Atomically thin 2D materials like graphene and MoS_2 have been extensively studied recently because of their promising applications in optoelectronics,[1−4] spintronics,[5−9] transparent and flexible devices.[10−15] Because of its remarkable properties, such as high carrier mobility and mechanical flexibility, graphene has been incorporated into nonvolatile memory structures serving as a floating gate[16,17] or a transparent channel.[18] However, because of its zero band gap,[19] the graphene channeled memory devices typically possess a low program/erase current ratio, which significantly hinders its application in nonvolatile memory devices. Unlike graphene, MoS_2 has a transition from indirect band gap (1.2 eV) to a direct band gap (1.8 eV) in monolayer.[20,21] Its field effect transistors[22] show a high mobility of 200 $cm^2\ V^{-1}\ s^{-1}$ with a high on/off ratio approximately 10^8. To potentially enhance the program/erase current ratio, attempts were made to replace graphene with MoS_2 as a channel material in a ferroelectric memory[23] or as a charge-trap layer in a graphene flash memory.[24] It was demonstrated that the monolayer MoS_2 is very sensitive to the presence of charges.[17] However, the relatively small memory window, the degraded mobility, and the insufficient trap capability in those devices require further improvement of the charge-trap stack in the MoS_2 memory devices.[25−27]

It is known that high-κ dielectrics can serve as excellent charge-trap layers due to their reduced coupling crosstalk, weak charge leakage and good scalability.[28,29] Recently, various kinds of high-κ dielectrics were investigated

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including HfO_2, TiO_2, HfAlO and so on,[30−35] among which the $Al_2O_3/HfO_2/Al_2O_3$ gate stack has been widely used because of its high transparency, extraordinary thermal stability and remarkable trap capability.[36−39] Previous studies have also shown that the high-κ dielectrics can greatly enhance the mobility of MoS_2 transistors.[22,40] Thus, we anticipate that the integration of MoS_2 with $Al_2O_3/HfO_2/Al_2O_3$ can significantly enlarge the memory window and enhance the device performance.

In this article, we demonstrate a nonvolatile dual-gate charge-trap memory based on MoS_2 and high-κ HfO_2. As expected, the device shows a substantial memory window originated from the superior trap capacity of the $Al_2O_3/HfO_2/Al_2O_3$ stack. A back-gate electrode was also used to tune the carrier density of MoS_2, giving rise to a systematic shift of the threshold voltage and a gate-tunable memory window, thus enabling multibit information storage. The application of the conventional $Al_2O_3/HfO_2/Al_2O_3$ gate stack renders a possibility for a massive production of high-performance MoS_2-based 2D memory devices.

RESULTS AND DISCUSSION

Few-layer MoS_2 is obtained through mechanical exfoliation from bulk MoS_2 crystals onto prepatterned SiO_2/Si substrates. The thickness of SiO_2 is 270 nm. Two Cr/Au electrodes of 12 nm/100 nm were deposited *via* e-beam evaporation to form source and drain contacts. Subsequently, the $Al_2O_3/HfO_2/Al_2O_3$ gate stack was grown *via* an atomic layer deposition (ALD) system with a layer thickness of 7/8/30 nm, respectively. More details of device fabrication process can be found in the Methods and in the Supporting Information (Figure S1). A typical device architecture is shown in Figure 1a (also see a SEM picture in Figure 1b inset). An applied top-gate voltage (V_{TG}) modulates the amount of charge stored in the HfO_2 charge-trap layer, causing the variation of the conductivity of the MoS_2 channel. A back-gate voltage (V_{BG}) was applied to the degenerately doped silicon substrate to tune the memory characteristics by systematically shifting the Fermi level of MoS_2. To check the gate modulation, $I-V$ curves at different top-gate voltage were measured (Figure 1b): the source-drain current (I_{DS}) varies linearly with source-drain voltage (V_{DS}), indicative of developing Ohmic contacts.[41,42] The zero-gate current is on the order of 250 nA at 40 mV bias, implying the total resistance of about 160 KOhm. Devices with different thickness of contact metal (Cr)[43] (Supporting Information Table S1) shows little difference on the zero-gate resistance after

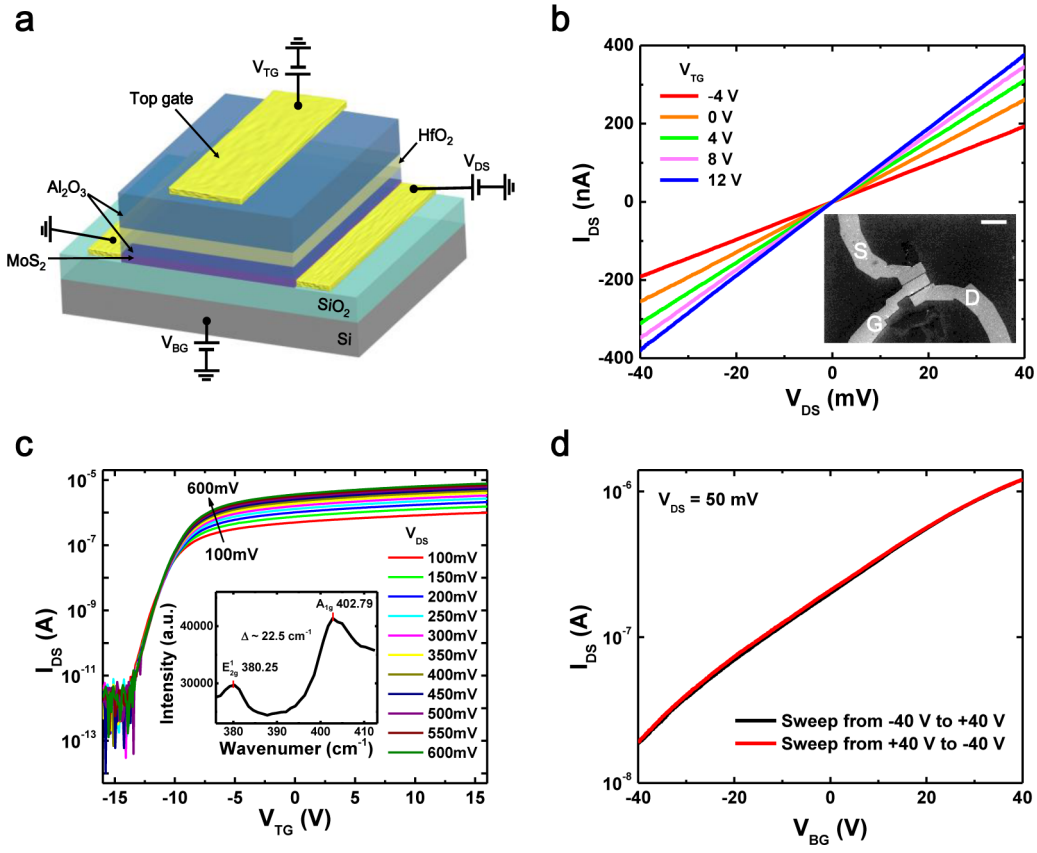

Figure 1. (a) Dual-gate device structure. The few-layer MoS_2 and 8 nm-thick HfO_2 serve as the channel and the trap layer, respectively. (b) The output characteristics ($I_{DS}-V_{DS}$) of the device under different top-gate voltage. The inset shows a scanning electron microscopy (SEM) image of the memory device. Scale bar, 10 μm. (c) Transfer curves of the device with the top gate. The inset shows a Raman spectrum of the MoS_2 used in the device, which is determined to be 3−4 layers. (d) $I_{DS}-V_{BG}$ curves of the device with the back-gate voltage sweeping back and forth between −40 and +40 V, showing negligible interface charge states.

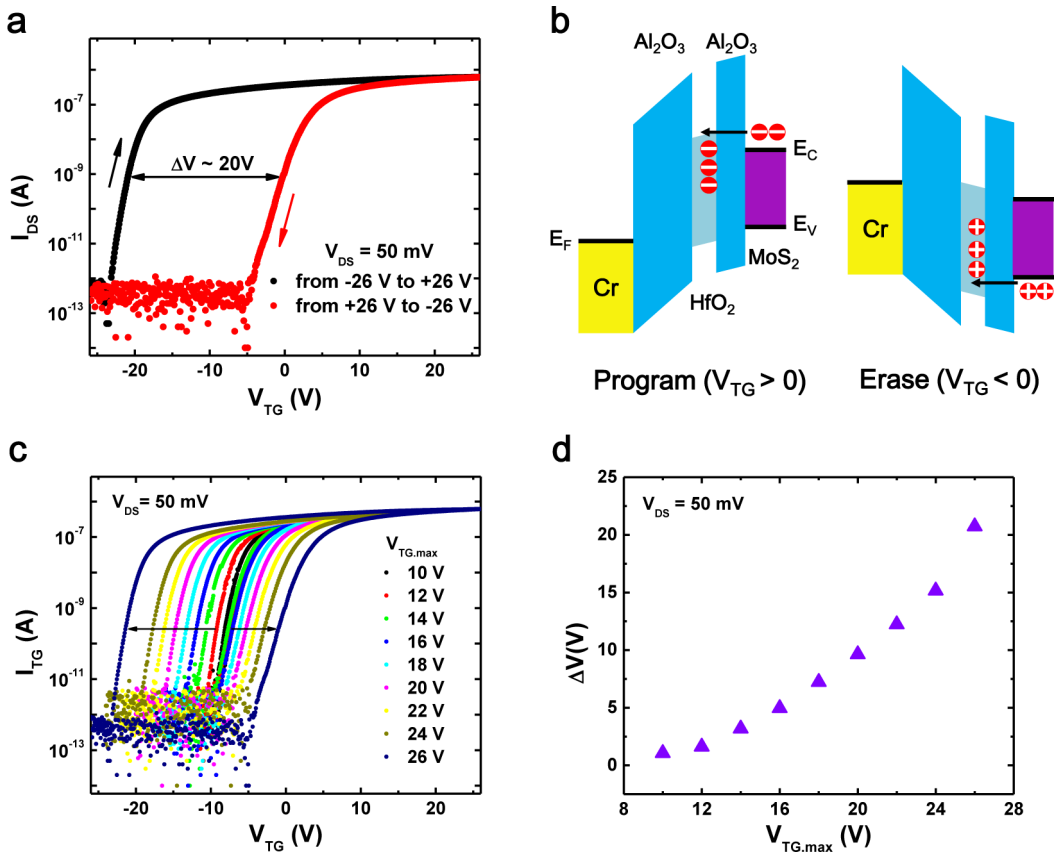

Figure 2. (a) Threshold voltage shift when sweeping V_{TG} from −26 to +26 V back and forth. The hysteresis of the transfer curves defines a memory window of ∼20 V. (b) Band diagram of the program/erase state of the device under positive and negative V_{TG}. Positive V_{TG} programs the device. Electrons tunneling from the few-layer MoS_2 channel are accumulated in the HfO_2 charge-trap layer. Negative V_{TG} erases the device. Holes tunnel from the few-layer MoS_2 channel to the HfO2 charge-trap layer. (c) $I_{TG}-V_{TG}$ characteristics under different $V_{TG.max}$ at V_{DS} = 50 mV. (d) Extraction of memory window *vs* $V_{TG.max}$. The memory window increases from ∼1 to ∼20 V in our experimental settings.

the ALD deposition (Supporting Information Figure S4). We noted that through the ALD deposition process the device performance can be significantly improved because of the thermal annealing under vacuum. Also, the encapsulation of MoS_2 in a high-κ dielectric environment will reduce the Coulomb scattering and modify the phonon dispersion in few-layer MoS_2.[44] The transfer curve ($I_{DS}-V_{TG}$) of the device can be obtained by sweeping V_{TG} while keeping the back gate grounded (Figure 1c). With V_{DS} gradually rising from 100 to 600 mV, a maximal on/off ratio higher than 10^5 was acquired. The MoS_2 in our device is measured to be about 3−4 layers by Raman spectroscopy (Figure 1c inset).[45] To elucidate the effect of interface charges on the device performance, it is necessary to measure the hysteresis behavior of $I_{DS}-V_{BG}$ (Figure 1d). When V_{BG} is swept between −40 and +40 V, the overlap of the forward and backward sweep curves shows a negligible interface effect from SiO_2 and the MoS_2 channel.[46]

The transfer characteristics were further explored to probe the storage capability of the MoS_2 memory device. As shown in Figure 2a, with V_{BG} = 0, V_{TG} was swept from −26 to +26 V and back to −26 V. A huge memory window of 20 V was observed, primarily originated from a large amount of electrons and holes stored in the HfO_2 charge-trap layer. Figure 2b illuminates the device operation process. When V_{TG} is swept toward a high positive value, electrons can tunnel through the 7 nm-thick Al_2O_3 barrier by means of Fowler−Nordheim tunneling.[47] The resultant accumulation of electrons in HfO_2 screens the top-gate electric field to reach the MoS_2 channel, which results in a positive shift of the threshold voltage (red curve in Figure 2a). When V_{TG} is swept from the positive to the negative direction, however, electrons are transferred back from the charge layer to the channel; simultaneously holes tunnel through the barrier and are trapped in the HfO_2 layer which causes the threshold shifting to the negative direction. The capability of electron and hole trapping leads to the appreciable memory window as large as 20 V, which is different from previously reported memory devices using monolayer MoS_2 as the channel.[17,24]

The amount of charge stored in the charge-trap layer can be modulated by gradually changing the maximum ($+V_{TG.max}$) and minimum ($-V_{TG.max}$) voltage applied on the top gate. Figure 2c shows the enlarged hysteresis window when $|V_{TG.max}|$ becomes larger.

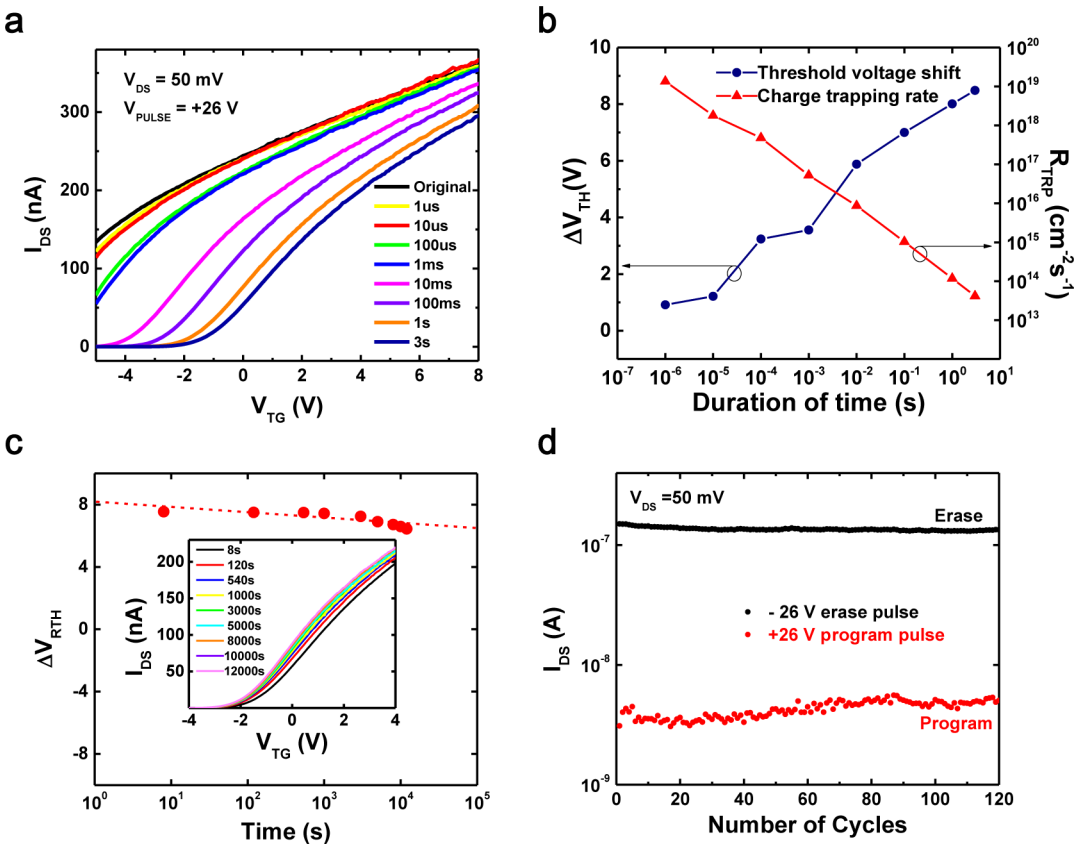

Figure 3. (a) Transfer curves of $I_{DS}-V_{TG}$ in a narrow range of $-5 \sim +8$ V under different pulse duration (1 μs to 3 s). (b) Extracted threshold voltage shift and calculated charge trap rate as a function of the pulse width. (c) Retention time of the threshold voltage. The programing pulse is set to be $+26$ V with 3 s duration. Inset shows the transfer curves ($I_{DS}-V_{TG}$) swept in different time intervals. Threshold voltage was obtained by linearly fitting to the transfer curves. We estimate that only 28% of the charges will be lost after 10 years. (d) Endurance of the memory device for 120 cycles with the program/erase voltage being $+26$ V, 200 ms duration and -26 V, 200 ms duration.

As aforementioned, the shift of the threshold voltage toward negative and positive direction corresponds to the hole and the electron trapping, respectively. The deduced threshold voltage shift (ΔV) as a function of $V_{TG.max}$ is summarized in Figure 2d. The amount of charge stored in the charge-trap layer can be estimated from the expression:[48]

$$n = \frac{\Delta V C_{HF-AL}}{e} \quad (1)$$

where e is the electron charge, ΔV is the threshold voltage shift toward the negative or the positive direction compare to the original transfer curve. According to Figure 2c,d, the hysteresis window of the sweep between -10 and $+10$ V is close to zero, thus it can be defined as the original transfer curve, corresponding to no tunneled electrons or holes existing in the charge-trap layer. $C_{HF-AL} = \varepsilon_0\varepsilon_{AL}/d_{AL}$ is the capacitance between the HfO_2 charge-trap layer and the top gate, where ε_0 is the vacuum permittivity, ε_{AL} and d_{AL} are the relative dielectric constant ($\sim$8) and thickness ($\sim$30 nm) of the Al_2O_3 blocking layer, respectively. The calculated density of stored electrons and holes is on the order of $\sim 8.6 \times 10^{13}$ and $\sim 1.9 \times 10^{14}$ cm^{-2}, respectively, which is in agreement with previously reported memory devices using graphene or graphene oxide as charge-trap layers.[16,49] The lower tunneling barrier height of holes than electrons is accounted for the high trap density of holes,[50] as detailed in the Supporting Information (Figure S2).

To study the dynamic transition rate of the MoS_2 memory device,[15,21] a negative pulse (-26 V, duration of 3 s) was applied to the top gate ($V_{BG} = 0$) to set the device in the erase state, followed by a $+26$ V pulse with different duration time. The reading procedure was performed by sweeping $I_{DS}-V_{TG}$ in a very small range (-5 to $+9$ V) to minimize the effect of the measurements to the device's state. After each reading operation, a negative pulse (-26 V, duration of 3 s) was applied on the top gate to reset the device in the erase state. The threshold voltage shift ΔV_{TH} was acquired by applying a linear fit to the linear regime of the reading $I_{DS}-V_{TG}$ curve. Figure 3a shows a clear shift of the threshold voltage when the width of the pulse is changed to 10 ms, which sets a reference for the following dynamic behavior measurements. ΔV_{TH} shows nearly a saturation behavior when the pulse width increases to 3 s (Figure 3a). The charge-trapping

rate can be estimated from the expression:[24]

$$[dN_{trap}/dt] = [C_{HF-AL}/e] \times [\Delta V_{TH}/\Delta t] \quad (2)$$

where ΔV_{TH} is the threshold voltage shift and Δt is the pulse width. The calculated charge-trapping rate varies from 10^{19} to 10^{14} cm^{-2} t^{-1} when the pulse width changes from 1 ms to 3 s. The reason for such a high charge-trap rate is because of the thin Al_2O_3 tunnel layer (only 7 nm), which makes electron/hole charges much easier to tunnel through.[51]

The retention characteristics of the device are determined by the height of the tunneling barrier and the depth of potential well formed in the $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack.[52] Figure 3c inset shows the threshold voltage at different time intervals after programming the device with a positive pulse (+26 V, duration of 3 s). To prevent perturbation of the measurements to the device state, the transfer curve was also obtained in a small voltage range (−4 to +4 V). The extracted threshold voltage ΔV_{RTH} varies from 7.5 to 6.4 V after 10^4 s (Figure 3c), from which we estimate that only ~28% of the charges will be lost after 10 years. The enhancement of the retention characteristics of our MoS_2 memory device is also related to the extraordinary trapping ability of the $Al_2O_3/HfO_2/Al_2O_3$ gate stack.[36,38] To test the endurance of the memory device, a sequence of pulse (±26 V, duration of 200 ms) was applied to the top gate with V_{BG} = 0 while I_{DS} was measured (V_{DS} = 50 mV). As presented in Figure 3d, the device is stable after 120 cycles. The robustness and stability of the device shows a great perspective of applications in nonvolatile memory technology.

Memory cells with tunable characteristics can be used in multioperational mode circuits where one device can show various functionalities.[53] To demonstrate such tunability, a back-gate voltage is applied to the MoS_2 channel and the transfer curves between −26 and +26 V were obtained under different V_{BG} (Figure 4). It is noted that the window size can be effectively tuned from 15.6 to 21 V with V_{BG} varying from +35 to −35 V (Figure 4 inset). The mechanism of the back-gate tunability can be qualitatively explained as follows: the negative V_{BG} moves the Fermi level of the MoS_2 approaching the middle of the bandgap and makes it more intrinsic, thus becoming sensitive to the charges stored in the charge-trap layer, which also results in its being easily turned off. On the contrary, the positive V_{BG} makes the MoS_2 channel highly doped and insensitive to the tunneling charges. The device is thus difficult to be switched off, leading to a smaller memory window.

To further investigate the tunability and the stability of the device under different back-gate voltage, the dynamic behavior was revisited. With V_{DS} = 50 mV, switching between the program and the erase state is achieved by applying negative and positive pulses to the top gate with different V_{BG}. As illustrated in Figure 5a,b,c, the device was set to a program state

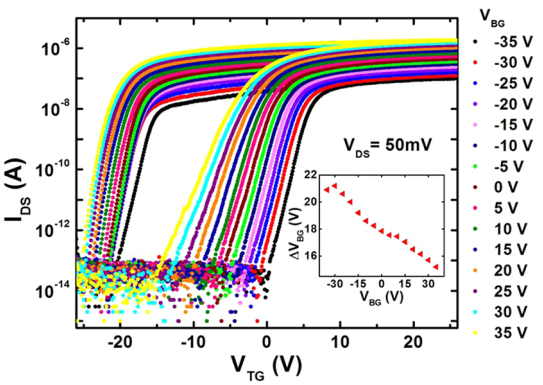

Figure 4. Top gate of the device was swept from −26 to +26 V back and forth under different V_{BG} ranging from −35 to +35 V. The inset summarizes the size of the memory window with respect to the V_{BG}.

when a +26 V pulse with an applied duration of 200 ms which makes the electrons accumulated in the charge-trap layer. We note that the charge density in the MoS_2 channel can suddenly increase during the positive pulse, as depicted by the source-drain current peak in Figure 5a,b,c. The device remains in the program state after the top-gate voltage is reset to 0 V; and the relatively low current corresponds to the device OFF state. After three seconds, a negative pulse (−26 V, 200 ms) is applied to set the device in the erase state. The high current reassembles the ON state. Importantly, there is no obvious decay or increase of the ON current, suggesting that the impact of the charge impurities present at the semiconductor/dielectric interface is relatively small.[17,46] The application of V_{BG} also leads to the change of the ON and OFF currents. When V_{BG} = −35 V, the MoS_2 channel becomes more intrinsic with a relatively low conductance thus the ON and OFF current is low (Figure 5a). In comparison, When V_{BG} =+35 V a high ON and OFF current level can be achieved as shown in Figure 5c.

The retention of the program/erase state of the device was also measured with V_{DS} = 50 mV under different V_{BG}. With a negative voltage pulse (−26 V, 3 s), the erase state current of the device was monitored in 2000 s. Subsequently, a positive voltage pulse (+26 V, 3 s) was applied to the top gate while the program current was recorded on the same time scale. Because of the back-gate voltage, we can tune the level of program and erase current, for instance, V_{BG} = −35 V enlarges the program/erase current ratio to the order of 10^4, making it easy for read-out; however, V_{BG} = +35 V can dramatically reduce the current ratio to be about 3, demonstrating a wide range of tunability. It should be noted that the devices with more than 4−5 layers MoS_2 always show reduced program/erase current ratios since the screening length of MoS_2 devices is about 3−5 nm,[54] When MoS_2 becomes thicker (6−7 layers of or even more) the top layers of MoS_2 screen the bottom layers from storing charges

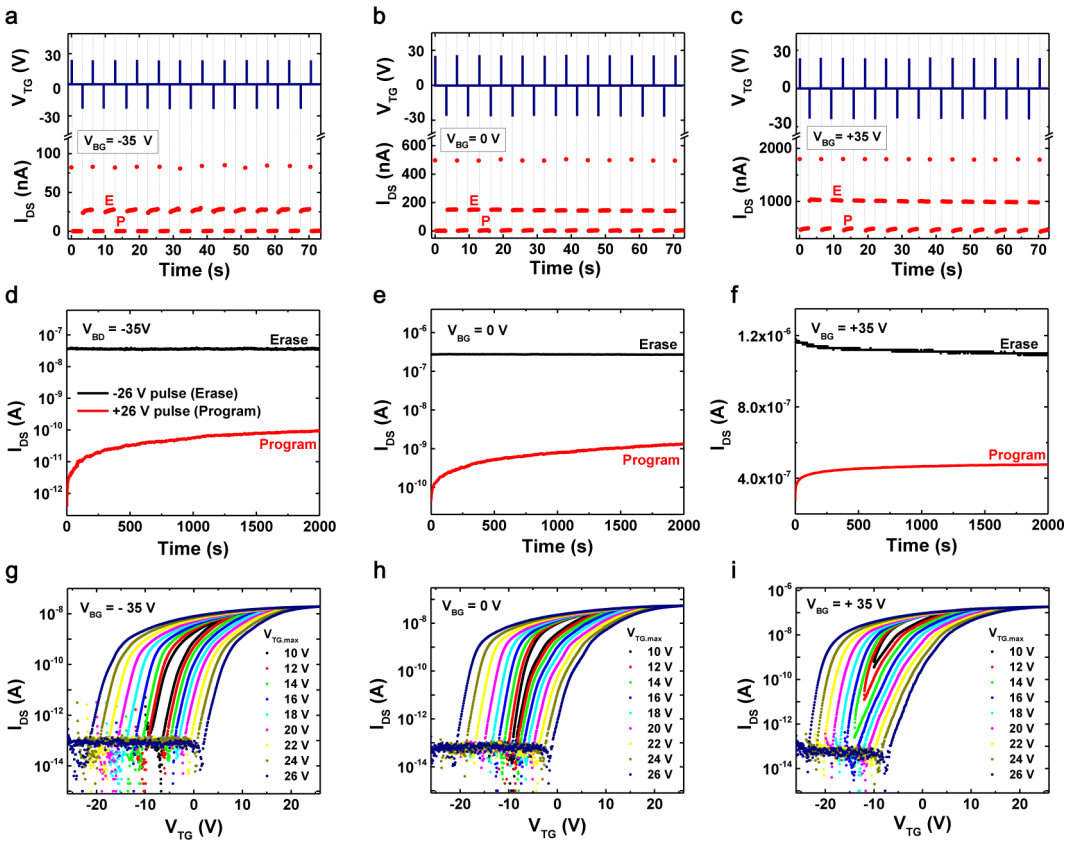

Figure 5. (a,b,c) The dynamic behavior of the device under a back-gate voltage of −35, 0 and +35 V, respectively. They were applied with a program voltage of +26 V (V_{TG}), 200 ms duration and an erase voltage of −26 V, 200 ms duration (V_{DS} = 50 mV). Negative back-gate voltage (−35 V) reduces the current levels of ON (Erase, device on) and OFF (Program, device off) states. In contrast, the positive back-gate voltage (+35 V) leads to higher ON and OFF current levels. (d,e,f) The stability of program/erase state of the device after programing at +26 V, 3 s duration and erasing at −26 V, 3 s duration (V_{DS} = 50 mV). The program/erase current ratio of the device varies from 3 to ~10^4 when the back-gate voltage changes from −35 to +35 V. (g,h,i) Significant change of the threshold voltage shift upon the application of the back-gate voltage (V_{DS} = 30 mV). The negative part of the threshold voltage shift corresponds to the hole trapping which can be suppressed by the positive back-gate voltage, vice versa for the electron trapping in the positive part.

thus making the program state current higher. Detailed analysis on thickness-dependent memory devices can be found in Supporting Information Table S1. Figure 5b,c,d also show six different current levels of the memory device and at least 2 bits can be stored in the memory device.[55] Compared to other multibit storage methods,[56] the different current levels tuned by the back gate in the MoS_2 memory device are more controllable and stable which may allow for future applications of large-scale MoS_2-based nonvolatile memory devices.

To verify the hole storage capability in the charge-trap layer, the top-gate voltage was swept from $-V_{TG.max}$ to $+V_{TG.max}$ under a specific V_{BG} of −35, 0, +35 V, as shown in Figure 5d,e,f, respectively. It is noted that the shift of the threshold voltage in the negative direction becomes smaller when V_{BG} increases to +35 V. This is because the positive V_{BG} electrostatically dopes the MoS_2 channel thus reducing the number of holes; so there are less holes tunneling though the barrier. The expansion of the memory window under V_{BG} of −35 V is consistent with the results form Figure 4, evidencing a strong capability of the hole storage in our memory device.

CONCLUSION

In summary, we have demonstrated a dual-gate charge-trap memory device based on few-layer MoS_2 and $Al_2O_3/HfO_2/Al_2O_3$ charge-trap stack. Utilizing a back-gate structure, the memory window and the program/erase current ratio can be efficiently modulated. The robustness and stability of the tunable MoS_2−HfO_2 memory is promising for multibit information storage.

METHODS

The drain-source electrodes of the device were fabricated by *e*-beam lithography (EBL) using PMMA/MMA bilayer polymer. Cr/Au (12 nm/100 nm) electrodes were deposited by *e*-beam evaporation. After lift-off, a 1 nm-thick Al layer was deposited and oxidized in the air for 24 h, acting as a seed layer for subsequent deposition of $Al_2O_3/HfO_2/Al_2O_3$ (7 nm/8 nm/30 nm)

via atomic layer deposition (ALD). During the ALD process, trimethylaluminum and trtrakis (ethyl-methylamido) hafnium were reacted at 200 °C with water for Al_2O_3 and HfO_2, respectively. The top-gate (Cr/Au 12 nm/100 nm) electrode was fabricated using another EBL and metal deposition process. Electrical properties of the fabricated devices were measured in a probe station using a semiconductor device parameter analyzer (Agilent, B1500A).

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Detailed procedures of the device fabrication; band diagram of the MoS_2 charge-trap device; $I_{DS}-V_{BG}$ of the MoS_2 charge-trap device; Transfer behavior of the MoS_2 charge-trap device before and after the ALD deposition; Gate leakage current of the MoS_2 charge-trap device; Performance of the devices with different device structures; "2-bit" storage measured with 24 h and methods of defining charge loss of 10 years; Detailed performance of other functioning devices. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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